CLAIMS

1. A method of adjusting data timing in a memory system having a memory device and a memory controller, the system operating according to a master clock signal, the method comprising the steps of:

establishing an initial output timing at the memory device;

transmitting a first set of data from the memory device to the memory controller according to the initial output timing;

transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing;

receiving the echo clock signal at the memory controller;

identifying a phase error of the received echo clock signal relative to the master clock signal;

revising the initial output timing in response to the identified phase error to produce a revised output timing; and

transmitting a second set of data from the memory device to the memory controller according to the revised output timing.

2. The method of claim 1 wherein the step of identifying a phase error of the received echo clock signal relative to the master clock signal comprises the steps of:

generating a plurality of phase shifted signals responsive to the master clock signal;

comparing the echo clock signal to each of the phase shifted signals; and

identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal.

3. The method of claim 2 wherein the step of establishing an initial output timing includes the steps of:

setting a delay of a delay circuit; and

applying the master clock signal to the delay circuit to produce the echo clock signal.

4. The method of claim 3 wherein the step of establishing an initial output timing further includes the steps of:

storing data in an output register;

clocking the register with the echo clock signal; and

outputting data from the register in response to the echo clock signal.

5. The method of claim 3 wherein the step of revising the initial output timing includes the step of adjusting the delay of the delay circuit.

6. A method of controlling data flow in a memory system including a memory controller and a memory device, the method comprising the steps of:

generating a master clock signal;

transmitting the master clock signal from the memory controller to the memory device;

issuing a first read command to the memory device;

reading a first set of data from the memory device in response to the read command;

producing an echo signal at the memory device in response to the first read command, the echo signal having a phase shift relative to the master clock signal;

transmitting the first set of data to the memory controller with a time delay relative to the echo signal;

transmitting the echo signal to the memory controller;

receiving the echo signal at the memory controller;

comparing the received echo signal to the master clock signal;

selecting an adjusted time delay in response to the step of comparing the received echo signal to the master clock signal;

issuing a second read command to the memory device;

reading a second set of data in response to the second read command; and

transmitting to the memory controller the second set of data with the adjusted time delay.

7. The method of claim 6 wherein the step of selecting an adjusted time delay includes the step of adjusting a vernier.

8. The method of claim 6 wherein the step of comparing the received echo signal to the master clock signal includes the steps of:

producing a plurality of phase-shifted signals in response to the master clock signal; and

comparing the echo signal to each of the phase-shifted signals.

9. The method of claim 8 wherein the step of selecting an adjusted time delay includes the step of identifying one of the phase-shifted signals closest in phase to the echo clock signal.

10. A memory controller for a memory system including a plurality of memory devices coupled to common clock and command busses, the memory devices producing echo signals in response to clock signals on the clock bus, the controller comprising:

a master clock source coupled to the clock bus operative to produce a master clock signal;

a phase comparing circuit coupled to the clock bus and responsive to produce a phase signal in response to a phase difference between the echo signal and the master clock signal;

a logic circuit coupled to the phase comparing circuit and adapted to produce adjustment data in response to the phase signal; and

a control data circuit having a command output coupled to the command bus and adapted to produce a command signal at the command output in response to the adjustment data.

11. The memory controller of claim 10 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the clock bus and a phase output coupled to the logic circuit.

12. The memory controller of claim 6 wherein the signal source includes a multiple output delay-locked loop.

13. A memory system, comprising:

a command bus;

a clock bus;

a data bus;

a memory controller including a master clock generator coupled to the clock bus, a phase comparator having a first input coupled to the master clock generator and a second input and responsive to a phase difference between the first and second inputs to produce an adjust command, and a logic circuit; and

a memory device having a clock input coupled to the clock bus, an echo signal generator responsive to the master clock signal at the clock input, the echo signal generator being coupled to the second input of the phase comparator, a data latch having a trigger input and responsive to a control signal at the trigger's input to transmit data to the data bus, and a variable delay circuit having a control output coupled to the trigger input and a command input coupled to the command bus, the delay circuit being responsive to the adjust command on the command bus to produce a delay corresponding to the adjust command.

14. The memory system of claim 13 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the clock bus and a phase output coupled to the logic circuit.

15. The memory system of claim 14 wherein the signal source includes a multiple output delay-locked loop.

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